***In the Claims*:**

Please cancel claims 1-111.

Please add new claims 112-132.

112. (New) A semiconductor structure comprising:

a layer structure including a uniform etch-stop layer,

wherein said uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

113. (New) The semiconductor structure of claim 112, wherein the uniform etch-stop layer is substantially relaxed.

114. (New) The semiconductor structure of claim 113, wherein the uniform etch-stop layer comprises $Si_{1-y}Ge_y$.

115. (New) The semiconductor structure of claim 114, wherein $y>0.19$.

116. (New) The semiconductor structure of claim 113, wherein the uniform etch-stop layer comprises a silicon dioxide layer.

117. (New) The semiconductor structure of claim 113, wherein a surface of the uniform etch-stop layer is planarized.

118. (New) The semiconductor structure of claim 112, wherein the layer structure comprises a strained layer disposed over the uniform etch stop layer.

119. (New) The semiconductor structure of claim 118, wherein the strained layer comprises $Si_{1-z}Ge_z$ and $0\leq z<1$.

120. (New) The semiconductor structure of claim 118, further comprising:

an insulator layer disposed over the layer structure.

121. (New) The semiconductor structure of claim 112, further comprising:
a handle wafer,
wherein the layer structure is bonded to the handle wafer.

122. (New) The structure of claim 121, wherein the handle wafer comprises an insulator.

123. (New) The semiconductor structure of claim 121, wherein the handle wafer comprises a material selected from the group consisting of silicon, glass, quartz, and silicon dioxide.

124. (New) The semiconductor structure of claim 123, wherein the handle wafer comprises a silicon dioxide layer.

125. (New) The semiconductor structure of claim 112, wherein the layer structure comprises a substantially relaxed layer.

126. (New) The semiconductor structure of claim 125, wherein the relaxed layer is graded.

127. (New) The semiconductor structure of claim 126, wherein the relaxed layer comprises $Si_{1-x}Ge_x$.

128. (New) The semiconductor structure of claim 127, wherein $x<0.2$.

129. (New) The semiconductor structure of claim 128, wherein the uniform etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$ and $y>0.19$.

130. (New) The semiconductor structure of claim 125, wherein the substantially relaxed layer is disposed over the uniform etch-stop layer.

131. (New) The semiconductor structure of claim 130, further comprising:
a semiconductor substrate disposed over the relaxed layer.

132. (New) The semiconductor structure of claim 125, wherein the substantially relaxed layer is disposed under the uniform etch-stop layer.

133. (New) The semiconductor structure of claim 132, wherein the layer structure comprises a first strained layer disposed over the uniform etch-stop layer.

134. (New) The semiconductor structure of claim 132, wherein the first strained layer comprises $Si_{1-z}Ge_z$ and $0 \leq z < 1$.

135. (New) A semiconductor structure, comprising:

a layer structure including a strained $Si_{1-z}Ge_z$ layer, and

a handle wafer comprising an insulator, the layer structure being bonded to the handle wafer,

wherein $0 \leq z < 1$.

136. (New) The semiconductor structure of claim 135, wherein $z=0$.

137. (New) The semiconductor structure of claim 135, wherein the layer structure includes a substantially relaxed uniform etch-stop layer, the strained $Si_{1-z}Ge_z$ layer is disposed over the uniform etch-stop layer, $0 \leq z < 1$, and the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

138. (New) The semiconductor structure of claim 137, wherein the etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

139. (New) The semiconductor structure of claim 137, wherein the layer structure comprises a substantially relaxed layer and the uniform etch-stop layer is disposed over the substantially relaxed layer.

140. (New) The semiconductor structure of claim 139, wherein the substantially relaxed layer comprises graded $Si_{1-x}Ge_x$.

141. (New) The structure of claim 139, further comprising:

an insulator layer disposed over the layer structure.

142. (New) The semiconductor structure of claim 139, wherein the layer structure comprises a substantially relaxed graded layer disposed over the substantially relaxed layer.

143. (New) The semiconductor structure of claim 142, wherein the substantially relaxed graded layer comprises $Si_{1-x}Ge_x$.

144. (New) A semiconductor structure, comprising:

a layer structure including:

a uniform etch-stop layer; and

a strained layer disposed over the uniform etch-stop layer, and

an insulator layer disposed over the layer structure,

wherein the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

145. (New) The semiconductor structure of claim 144, wherein the etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

146. (New) The semiconductor structure of claim 144, wherein the strained layer comprises $Si_{1-z}Ge_z$ and $0 \leq z < 1$.

147. (New) A semiconductor structure, comprising:

an etch-stop layer; and

a substantially relaxed layer disposed over the etch-stop layer.

148. (New) The semiconductor structure of claim 147, wherein the etch-stop layer comprises strained $Si_{1-z}Ge_z$ and $0 \leq z < 1$.

149. (New) The semiconductor structure of claim 148, wherein $z=0$.

150. (New) The semiconductor structure of claim 147, wherein the substantially relaxed layer comprises $Si_{1-w}Ge_w$.

151. (New) A semiconductor structure, comprising:

a first uniform etch-stop layer;

a second etch-stop layer disposed over the uniform etch-stop layer; and

a substantially relaxed layer disposed over the second etch-stop layer,

wherein the first uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

152. (New) The semiconductor structure of claim 151, wherein the first uniform etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

153. (New) The semiconductor structure of claim 151, wherein the second etch-stop layer comprises strained $Si_{1-z}Ge_z$.

154. (New) The structure of claim 153, wherein $0 \leq z < 1$.

155. (New) The semiconductor structure of claim 154, wherein $z=0$.

156. (New) The semiconductor structure of claim 151, wherein the substantially relaxed layer comprises $Si_{1-w}Ge_w$.

157. (New) The semiconductor structure of claim 151, further comprising:

a handle wafer comprising an insulator,

wherein the substantially relaxed layer is bonded to the handle wafer.

158. (New) The semiconductor structure of claim 157, wherein the handle wafer comprises a material selected from the group consisting of silicon, glass, quartz, and silicon dioxide.

159. (New) The semiconductor structure of claim 157, further comprising:

an insulator layer disposed over the strained layer.

160. (New) The semiconductor structure of claim 151, further comprising:

a substantially relaxed graded layer,

wherein the first uniform etch-stop layer is disposed over the graded layer.

161. (New) The semiconductor structure of claim 160, wherein the substantially relaxed graded layer comprises $Si_{1-x}Ge_x$.

162. (New) The semiconductor structure of claim 160, further comprising:

a first substrate,

wherein the substantially relaxed graded layer is disposed on the first substrate.

163. (New) A method for forming a semiconductor structure, the method comprising:

forming a uniform etch-stop layer;

providing a handle wafer; and

bonding the uniform etch-stop layer to the handle wafer,

wherein said uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

164. (New) The method of claim 163, wherein the uniform etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

165. (New) The method of claim 163, further comprising:

planarizing a surface of the uniform etch-stop layer prior to bonding.

166. (New) The method of claim 163, further comprising:

forming a substantially relaxed graded layer before forming the uniform etch-stop layer,

wherein the uniform etch-stop layer is formed over the substantially relaxed graded layer.

167. (New) The method of claim 166, wherein the relaxed graded layer comprises $Si_{1-x}Ge_x$.

168. (New) The method of claim 166, further comprising:

releasing the etch-stop layer by removing at least a portion of the graded layer.

169. (New) The method of claim 166, wherein releasing the etch-stop layer comprises a wet etch.

170. (New) The method of claim 166, further comprising:

providing a semiconductor substrate,

wherein the substantially relaxed graded layer is formed over the semiconductor substrate.

171. (New) A method for forming a semiconductor structure, the method comprising:

providing a first substrate; and

forming a layer structure over the first substrate by:

forming a uniform etch-stop layer over the first substrate; and

forming a strained layer over the uniform etch-stop layer,

wherein the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

172. (New) The method of claim 171, wherein the etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

173. (New) The method of claim 171, wherein the strained layer comprises $Si_{1-z}Ge_z$ and $0 \leq z < 1$.

174. (New) The method of claim 171, further comprising:

providing a second substrate comprising an insulator; and

bonding the layer structure to the second substrate.

175. (New) The method of claim 174, wherein the second substrate comprises a material selected from the group consisting of silicon, glass, quartz, and silicon dioxide.

176. (New) The method of claim 171, further comprising:

forming an insulator layer over the strained layer.

177. (New) The method of claim 171, further comprising:
releasing the strained layer by removing at least a portion of the uniform etch-stop layer.

178. (New) The method of claim 177, wherein releasing the strained layer comprises a wet etch.

179. (New) The method of claim 171, wherein forming the layer structure comprises forming a substantially relaxed graded layer and the uniform etch-stop layer is formed over the graded layer.

180. (New) The method of claim 179, wherein the graded layer comprises $Si_{1-x}Ge_x$.

181. (New) The method of claim 179, further comprising:
releasing the strained layer by removing at least a portion of the graded layer and at least a portion of the uniform etch-stop layer.

182. (New) The method of claim 181, wherein releasing the strained layer comprises a wet etch.

183. (New) A method for forming a semiconductor structure, the method comprising:
forming a layer structure by forming a strained $Si_{1-z}Ge_z$ layer, and
bonding the layer structure to a handle wafer comprising an insulator,
wherein $0 \leq z < 1$.

184. (New) The method of claim 183, wherein $z=0$.

185. (New) The method of claim 183, wherein forming the layer structure comprises forming a uniform etch-stop layer, the strained $Si_{1-z}Ge_z$ layer is formed over the uniform etch-stop layer, and the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

186. (New) The method of claim 185, wherein the uniform etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

187. (New) The method of claim 185, further comprising:
forming an insulator layer over the layer structure.

188. (New) The method of claim 185, further comprising:
releasing the strained layer by removing at least a portion of the uniform etch-stop layer.

189. (New) The method of claim 188, wherein releasing the strained layer comprises a wet etch.

190. (New) The method of claim 185, wherein forming the layer structure comprises forming a substantially relaxed graded layer, and the uniform etch-stop layer is formed over the substantially graded layer.

191. (New) The method of claim 190, wherein the relaxed graded layer comprises $Si_{1-x}Ge_x$.

192. (New) The method of claim 190, further comprising:
releasing the strained layer by removing at least a portion of the graded layer and at least a portion of the uniform etch-stop layer.

193. (New) The method of claim 192, wherein releasing the strained layer comprises a wet etch.

194. (New) The method of claim 190, further comprising:
forming an insulator layer over the layer structure.

195. (New) The method of claim 190, further comprising:
providing a substrate,
wherein the layer structure is formed over the substrate.

196. (New) The method of claim 195, further comprising:

releasing the strained layer by removing at least a portion of the substrate, at least a portion of the graded layer, and at least a portion of the uniform etch-stop layer.

197. (New) The method of claim 196, wherein releasing the strained layer comprises a wet etch.

198. (New) A method for forming a semiconductor structure, the method comprising:
forming a strained etch-stop layer; and
forming a substantially relaxed $Si_{1-w}Ge_w$ layer over the etch-stop layer.

199. (New) The method of claim 198, wherein the etch-stop layer comprises $Si_{1-z}Ge_z$ and wherein $0 \leq z < 1$.

200. (New) The method of claim 199, wherein $z=0$.

201. (New) A method for forming a semiconductor structure, the method comprising:
forming a first uniform etch-stop layer;
forming a second etch-stop layer over the uniform etch-stop layer; and
forming a substantially relaxed layer over the second etch-stop layer,
wherein the first uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

202. (New) The method of claim 201, wherein the first etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

203. (New) The method of claim 201, wherein the second etch-stop layer comprises strained $Si_{1-z}Ge_z$ and $0 \leq z < 1$.

204. (New) The method of claim 203, wherein $z=0$.

205. (New) The method of claim 201, wherein the substantially relaxed layer comprises $Si_{1-w}Ge_w$.

206. (New) The method of claim 201, further comprising:

bonding the substantially relaxed layer to a substrate comprising an insulator.

207. (New) The method of claim 206, wherein the substrate comprises a material selected from the group consisting of silicon, glass, quartz, and silicon dioxide.

208. (New) The method of claim 206, further comprising:

releasing the second etch-stop layer by removing at least a portion of the first etch-stop layer.

209. (New) The method of claim 208, wherein releasing the second etch-stop layer comprises a wet etch.

210. (New) The method of claim 208, further comprising:

releasing the substantially relaxed layer by removing at least a portion of the second etch-stop layer.

211. (New) The method of claim 208, wherein releasing the substantially relaxed layer comprises a wet etch.

212. (New) The method of claim 201, further comprising:

forming a substantially relaxed graded layer,

wherein the first uniform etch-stop layer is formed on the graded layer.

213. (New) The method of claim 212, wherein the substantially relaxed graded layer comprises $Si_{1-x}Ge_x$.

214. (New) The method of claim 212, further comprising:

bonding the substantially relaxed layer to a substrate comprising an insulator.

215. (New) The method of claim 212, further comprising:

releasing the first etch-stop layer by removing at least a portion of the relaxed graded layer.

216. (New) The method of claim 215, wherein releasing the first etch-stop layer comprises a wet etch.

217. (New) The method of claim 215, further comprising:

releasing the second etch-stop layer by removing at least a portion of the first etch-stop layer.

218. (New) The method of claim 215, wherein releasing the second etch-stop layer comprises a wet etch.

219. (New) The method of claim 217, further comprising:

releasing the relaxed layer by removing at least a portion of the second etch-stop layer.

220. (New) The method of claim 219, wherein releasing the relaxed layer comprises a wet etch.

221. (New) The method of claim 201, further comprising:

providing a first substrate; and

forming a layer structure over the first substrate by:

forming a substantially relaxed graded layer over the first substrate;

wherein the first uniform etch-stop layer is formed over the graded layer, and the layer structure comprises the substantially relaxed graded layer, the first uniform etch-stop layer, the second etch-stop layer, and the substantially relaxed layer.

222. (New) The method of claim 221, wherein the substantially relaxed graded layer comprises $Si_{1-x}Ge_x$.

223. (New) The method of claim 221, wherein the first uniform etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$, the second etch-stop layer comprises strained $Si_{1-z}Ge_z$, $0 \leq z < 1$, and the substantially relaxed layer comprises $Si_{1-w}Ge_w$.

224. (New) The method of claim 221, further comprising:

bonding the layer structure to a second substrate including an insulator.

225. (New) The method of claim 224, wherein the second substrate comprises a material selected from the group consisting of silicon, glass, quartz, and silicon dioxide.

226. (New) The method of claim 221, the method further comprising:

releasing the first etch-stop layer by removing at least a portion of the first substrate and at least a portion of the graded layer; and

releasing the second etch-stop layer by removing at least a portion of the first etch-stop layer.

227. (New) The method of claim 226, further comprising:

bonding the layer structure to a second substrate prior to releasing the first etch-stop layer.

228. (New) The method of claim 226, further comprising:

releasing at least a portion of the relaxed layer by removing at least a portion of the second etch-stop layer.

229. (New) A method for forming a semiconductor structure, the method comprising:

providing a first substrate;

forming a layer structure on the first substrate by:

forming a substantially relaxed graded layer on the first substrate; and

forming a uniform etch-stop layer on the graded layer; and

releasing the etch-stop layer by removing at least a portion of the substrate and at least a portion of the graded layer,

wherein the uniform etch-stop layer of $Si_{1-y}Ge_y$ has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

230. (New) The method of claim 229, wherein the substantially relaxed graded layer comprises $Si_{1-x}Ge_x$.

231. (New) The method of claim 229, wherein the uniform etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

232. (New) The method of claim 229, further comprising:

bonding the layer structure to a second substrate prior to releasing the etch-stop layer.

In the Abstract:

On page 46, after the heading "ABSTRACT," please rewrite the paragraph on lines 2-23 as:

A semiconductor structure including a uniform etch-stop layer. The uniform etch stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3. A method for forming a semiconductor structure includes forming a uniform etch-stop layer providing a handle wafer, and bonding the uniform etch-stop layer to the handle wafer. The uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

REMARKS

Claims 1-111 were originally filed in an earlier application to which priority is claimed. Applicants canceled without prejudice claims 1-111 and added new claims 112-232. Claims 112-232 will be pending after entry of this Amendment. Support for the new claims may be found *inter alia*, in the originally filed claims; on pages 5-31; and in the figures.

In addition, Applicants have amended the specification to include a specific reference to an earlier filed application for which the benefit of its filing date is claimed under 35 U.S.C. 120.